REMARKS

Claims 1-22 were pending in this application.

Claims 1-22 have been rejected.

No claims have been amended.

Claims 1-22 remain pending in this application.

Reconsideration and full allowance of Claims 1-22 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-22 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to Greenley et al. ("*Greenley*") in view of U.S. Patent No. 5,619,668 to Zaidi ("*Zaidi*"). The Applicant respectfully traverses this rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability,

then without more the Applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on the Applicant's disclosure. (*MPEP § 2142*).

Regarding Claims 1 and 14, the Office Action acknowledges that *Greenley* fails to disclose the use of "bypass circuitry" that is capable of "transferring [a] data value from [a] data cache directly to [a] target register without processing [the] data value in [a] shifter circuit" as recited in Claims 1 and 14. (*Office Action, Page 4, Paragraph 9b*). The Office Action then asserts that *Zaidi* discloses these elements of Claims 1 and 14 and that it would be obvious to modify *Greenley* with *Zaidi*. (*Office Action, Page 4, Paragraph 10b*).

First, the bypass mechanism of *Zaidi* fails to disclose, teach, or suggest the "bypass circuitry" recited in Claims 1 and 14. In particular, the bypass mechanism of *Zaidi* fails to

disclose, teach, or suggest "bypass circuitry" capable of transferring a data value from a "data cache directly to [a] target register" as recited in Claims 1 and 14.

The bypass mechanism of *Zaidi* simply takes data from a "source other than [a] register file" and provides the data as input to an arithmetic and logic unit ("ALU") 12. (*Abstract*). The bypass mechanism of *Zaidi* never transfers data from a data cache "directly to [a] target register." In fact, the bypass mechanism of *Zaidi* is specifically designed to bypass a register file 13, not to provide data from a data cache "directly to" the register file 13.

Second, the Office Action's proposed motivation for modifying *Greenley* with *Zaidi* actually teaches away from the claimed invention. The Office Action notes that a person skilled in the art would have recognized that the bypass mechanism of *Zaidi* "increases the speed of microprocessors ... by eliminating the time required to read data from the registers and aligning the data, and reduces the need to stall pipelines." (*Office Action, Pages 4-5, Paragraph 11*).

If anything, this motivation would lead a person skilled in the art to bypass writing data into a register of a register file. However, Claims 1 and 14 specifically recite that "bypass circuitry" functions to transfer a data value "from [a] data cache directly to [a] target register." As a result, the Office Action provides a motivation to avoid writing data to a register, which teaches away from the claimed "bypass circuitry" recited in Claims 1 and 14.

Third, the Office Action does not establish that the proposed modification of *Greenley* with the system of *Zaidi* would disclose, teach, or suggest all elements of Claims 1 and 14. *Zaidi* is specifically designed to reduce pipeline stalls caused by delays in waiting for data (such as the output of the ALU 12) to be written to the register file 13. The bypass mechanism of *Zaidi*

operates to provide the needed data directly to the input of the ALU 12, without waiting for the data to be written to the register file 13.

Modifying *Greenley* with *Zaidi* would not render Claims 1 and 14 obvious. *Greenley* retrieves data from a data cache 180, aligns the data in aligning unit 170, sign extends the data in sign extension unit 160, and stores the data in register files 150 for use by a processor 100. Implementing the bypass mechanism of *Zaidi* in *Greenley* would not bypass the aligning unit 170 and sign extension unit 160 of *Greenley* in order to store data in the register file 150. Instead, the bypass mechanism of *Zaidi* would bypass storing data in the register files 150 and provide the data directly to the processor 100. This would allow the processor 100 to use the data without waiting for the data to be written to the register files 150 of *Greenley*. In this proposed combination, data would not be transferred from the data cache 180 of *Greenley* "directly to" the register files 150 of *Greenley* using the bypass mechanism of *Zaidi*.

Because of this, the proposed *Greenley-Zaidi* combination fails to disclose, teach, or suggest "bypass circuitry" capable of "transferring [a] data value from [a] data cache directly to [a] target register without processing [the] data value in [a] shifter circuit" as recited in Claims 1 and 14. As a result, the proposed *Greenley-Zaidi* combination fails to disclose, teach, or suggest the Applicant's invention as recited in Claims 1 and 14 (and their dependent claims).

Claim 10 recites transferring a "data value from [a] data cache directly to [a] target register" without processing the data value in a "shifter circuit." As shown above, the proposed *Greenley-Zaidi* combination fails to disclose, teach, or suggest these elements of Claim 10. As a result, the proposed *Greenley-Zaidi* combination fails to disclose, teach, or suggest the

Applicant's invention as recited in Claim 10 (and its dependent claims).

For these reasons, the Office Action has not established a *prima facie* case of obviousness against Claims 1, 10, and 14 (and their dependent claims). Accordingly, the Applicant respectfully requests withdrawal of the § 103 rejection and full allowance of Claims 1-22.

II. CONCLUSION

The Applicant respectfully asserts that all pending claims in this application are in condition for allowance and respectfully requests full allowance of the claims.

SUMMARY

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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